MPD MICROWAVE PRODUCT DIGEST

FEATURED ARTICLES

October 24, 2016 mpdigest

Automated Circuit Synthesis and Simulation in RF Design Software

by Dale D. Henkes, ACS

The state of the art in RF circuit design today is greatly enhanced by a number of advanced computer aided engineering (CAE) software tools.

Most of the RF CAE software packages currently on the market provide circuit simulation in the frequency or time domain or both. Thus, the circuit simulator is generally the core product upon which other CAE software tools are added, usually for an additional cost. But circuit simulation is analysis, not design.

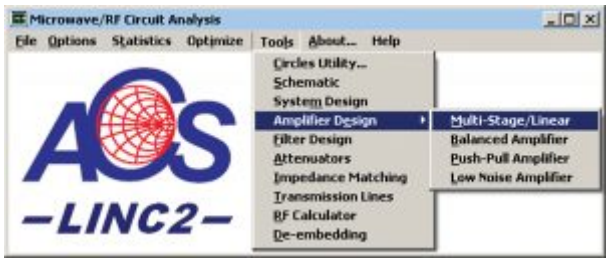

Figure 1: The LINC2 Tools Menu

The circuit simulator can take a circuit schematic and generate all kinds of performance analyses. However, simulation alone generally cannot suggest ways to change the circuit topology in order to improve performance or meet the desired specification more effectively, unless by rote trial and error. And where does the circuit come from that is presented to the simulator in the first place? The circuit can be manually created by the designer who has previous experience in the design of certain kinds of circuits or it can be designed by computer automation. We might call the latter approach true electronic design automation or EDA.

Circuit simulation, verification through statistical analysis (such as Monte Carlo simulation) and physical layout represent the back end of the design process. In recent years, a great deal of advancement has been made in EDA software that addresses the front end of the design process, i.e., in circuit synthesis software. Circuit synthesis programs can provide the highest level of design automation because they can take design specifications as input from the designer and automatically produce a schematic that captures the given design requirements.

The LINC2 Pro design automation software from ACS offers a comprehensive suite of automatic circuit synthesis software. Perhaps the most ubiquitous and well known form of circuit synthesis software is filter synthesis. Most RF engineers will recognize the familiar user interface of the typical filter synthesis program; how a filter type and topology is selected and frequency response specifications are entered. The essential form and flow of the filter synthesis user interface can be used in the automated synthesis of other circuits,

such as amplifiers and impedance matching networks. LINC2's extensive list of circuit and component synthesis includes, but is not limited to, the following:

- Lumped and distributed impedance matching networks that match real or complex source and load impedances
- Resonators, including special high Q transmission line resonators (in microstrip or stripline with modeled losses)
- Balanced and unbalanced attenuators
- Directional couplers
- BALUNS
- Low Noise Amplifier (LNA) design using lumped or distributed components
- Single and multi-stage amplifiers designed for balanced and unbalanced terminations
- Single and multi-stage balanced amplifiers (quad combined)
- Single and multi-stage push-pull amplifiers
- All matched to the user's choice of real or complex source and load impedances

Because impedance matching is so fundamental to the successful performance of RF and microwave circuits, LINC2 includes a synthesis package devoted entirely to the design of impedance matching networks.

This full-featured synthesis tool recognizes the modern trend for RF circuits to commonly employ balanced topologies that interconnect with RF ICs (RF integrated circuits) with differential ports. Thus, the LINC2 matching network tool synthesizes balanced matching networks as well as BALUN circuits for transforming between balanced and unbalanced circuits while simultaneously providing the required impedance match. The LINC2 filter synthesis program also designs balanced filters with differential ports.

Even the LINC2 attenuator design tool can synthesize balanced and unbalanced attenuators for equal or unequal terminations. The LINC2 amplifier design package also provides the option of incorporating the topology for balanced terminations into amplifier synthesis. LINC2 Amp Pro can design amplifiers with balanced ports for stand-alone push-pull operation or for direct insertion between differential circuits.

In this article we will look at three key components in a complete RF EDA software package: Circuit simulation, automatic circuit synthesis and circuit optimization.

This article will demonstrate how LINC2 can help the designer to:

1. Create the initial circuit design from a given set of design requirements or goals
2. Analyze the circuit with a circuit simulator
3. Optimize the circuit
4. Verify that the circuit can perform as required when component values vary over their full tolerance ranges

Broadband Amplifier Synthesis Design Example
The design of a two-stage amplifier will be presented here to illustrate the process. A few target specifications will serve as design goals for the LINC2 Pro amplifier synthesis module:

- Amplifier topology: Single-ended multi-stage linear amplifier
- Device: Wideband NPN bipolar low noise transistor (NXP BFR520)
- Gain: 27 +/- 0.5 dB
- Bandwidth (1 dB): 625 MHz to 1250 MHz (one octave BW)
- Distributed input and output matching networks: Microstrip

Creating the Initial Circuit Design: Synthesis
LINC2 amplifier synthesis is started by selecting Amplifier Design > Multi-Stage/Linear from the Tools menu (**Figure 1**). This action pops up the Design Specifications Form as shown in **Figure 2**. The Design Specifications Form allows the user to control the details of various aspects of the design. The user can specify the frequency, port impedances, stability criteria, topology and type of input and output matching networks (such as whether to use lumped or distributed networks), device selection and the interstage matching network if a multi-stage design is selected.

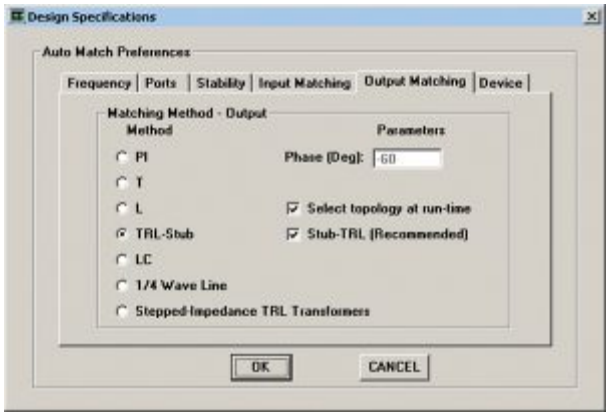

Figure 2: LINC2 design specifications form

Figure 3: LINC2 amplifier synthesis device and interstage matching selection

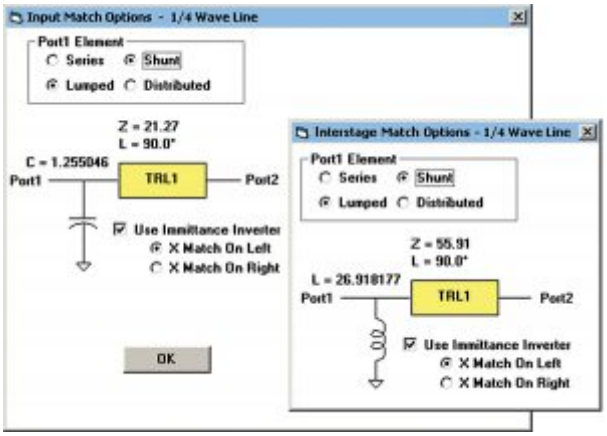

Figure 4: LINC2 port and interstage matching details

For this example two identical BFR520 NPN transistors will be used. The maximum available gain (MAG) for each transistor is about 13.6 dB at the highest frequency point in the design, so two in cascade will produce the desired 27 dB of gain. Thus, the Frequency tab is selected and 1250 MHz is entered as the design frequency for MAG. The default values for port impedances (50 ohms) are accepted. The defaults for stability considerations are also accepted. In this case the devices are unconditionally stable at the design frequency. However, if the active device selected was potentially unstable, then this tool can direct the program to automatically stabilize the device during circuit synthesis.

A number of lumped and distributed networks are available for matching port impedances to the device. In keeping with our design goals, distributed networks are selected for input and output matching. Both series and shunt transmission lines (TRL-Stub), quarter wave lines, or stepped-impedance transmission lines (TRL Transformers) are among the available options.

In this example, the Stub-TRL method was chosen for the output match (**Figure 2**). A quarter-wave line was selected from the options under the Input Matching tab. Checking "Select topology at run-time" provides more control over the design by allowing for more details about a particular topology to be specified during the synthesis process. One of the additional ways in which the user can guide the design is in the choice of the frequency response of the matching networks (low-pass, high-pass or bandpass). In this design, networks are chosen so as to produce a low-pass response for the overall two-stage amplifier. This helps to flatten the frequency response and delivers the additional benefit of suppressing harmonics.

The Device tab (**Figure 3**) defines the number of stages as equal to the number of devices selected (in this case, two). Each stage can be assigned a unique device (transistor). However, this particular design will use the same BFR520 transistor for each stage.

Device interstage matching choices are also found under the Device tab. Clicking on the interstage matching option box opens up a list of up to nine different interstage matching methods. Here the quarter-wave line (bottom of **Figure 3**) was selected from the pull-down menu list. The quarter-wave line (plus additional reactance/components specified later) will match the output of the first device to the input of the second device. Clicking OK at this point starts the amplifier synthesis.

After selecting the general topology of the input, output and interstage matching networks, the complete two-stage amplifier schematic would have immediately appeared upon clicking OK. But in this case we elected to make a couple of additional decisions regarding the application of components designed to make the quarter-wave lines more effective in the presence of complex impedances (**Figure 4**).

Lumped or distributed elements in series or shunt orientation can be applied at the device terminals to cancel the device reactances as shown in **Figure 4**. Moreover, the user can place the reactance on the left, right or on both sides of the quarter-wave line by simple selection of an immittance inverter.

Specifying this level of design detail for the matching networks is optional since the program can be directed to automatically synthesize the port and interstage matching without prompting the user for input. However,

"Select topology at run-time" gives the user more control over the amplifier's frequency response (among other things), directing the design toward a low-pass, high-pass or bandpass response. Clicking OK to accept the matching topology automatically generates the schematic for the two stage amplifier shown in **Figure 5**.

Optimizing the Amplifier for Broadband Response

A goal for this amplifier is to achieve 27 dB of gain over one octave of bandwidth covering the frequency range from 625 MHz to 1250 MHz. The goal for gain flatness is that the peak to peak gain ripple should be no more than 1 dB (for 27 dB +/- 0.5 dB over the specified bandwidth).

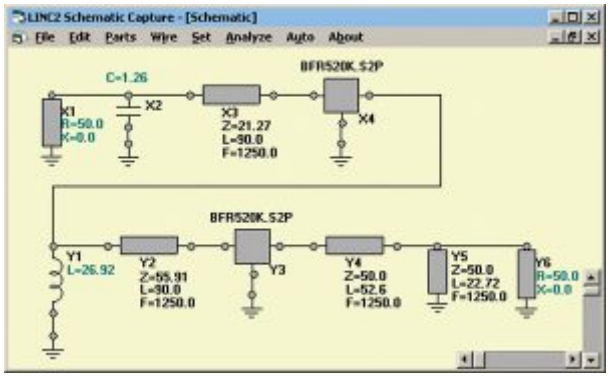

Figure 5: LINC2 synthesized amplifier schematic

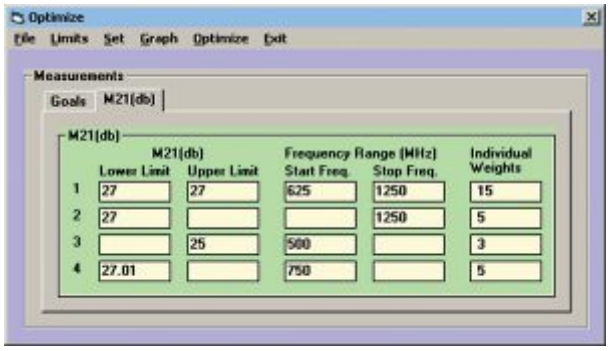

Figure 6: LINC2 optimizer goals

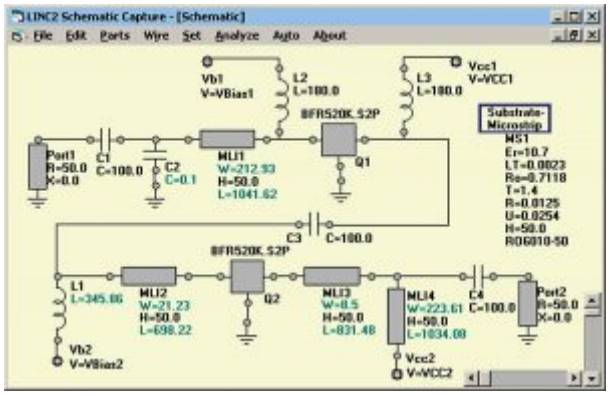

Figure 7: Optimized LINC2 amplifier schematic

Running a simulation of the synthesized schematic (**Figure 5**) shows that without optimization, the gain peaks at the high end of the band to the desired 27 dB but rolls off at the low end. However, before employing the optimizer to flatten the gain we convert all the ideal TRL (transmission line elements characterized by their impedance and electrical length) to physical microstrip. Fortunately, this process is also completely automated in LINC2. Clicking Auto > Convert T-Lines to > Microstrip requires only that we specify the substrate material. In this case we choose 50 mil Rogers RT/duroid® 6010 laminate. The schematic, with all lines converted to microstrip and bias feeds added, is shown in **Figure 7** (after optimization).

The design is now ready to optimize. The optimization goals are entered as shown in **Figure 6**. To flatten the gain we made the lower limit equal to the upper limit (setting each to 27 dB). After optimizing, the optimized component values are saved into the schematic (**Figure 7**). **Figure 8** shows the optimized frequency response. The simulation results plotted in the graph of **Figure 8** indicate that the gain meets the goal of 27 +/- 0.5 dB over the octave bandwidth from 625 MHz to 1250 MHz.

Circuit Performance Verification

LINC2 statistical yield analysis employs Monte Carlo simulations to determine the likely yield for a large number of samples. The goals for the desired outcome are entered as shown in **Figure 9**. Minimum values, maximum values or both can be entered for any design goal, and the frequency range over which the goal applies can be specified. In this case, we have specified the goal that the magnitude of S21 should remain within a 1.5 dB window about 27 dB.

All components selected for tuning or optimization are listed in the Tolerances menu. The default tolerance is +/- 5%, but each component parameter can be selected individually from the menu and its tolerance can be changed to any other value. The tolerance value for all components can be set to any range by selecting Reset Tolerances from the Set menu. In this example, the range for all microstrip dimensions (length and width) is set to +/- 2% for a total dimensional tolerance range of 4%. The capacitor and inductor values were also set to +/- 2%.

Figure 8: Gain response for the LINC2 designed amplifier

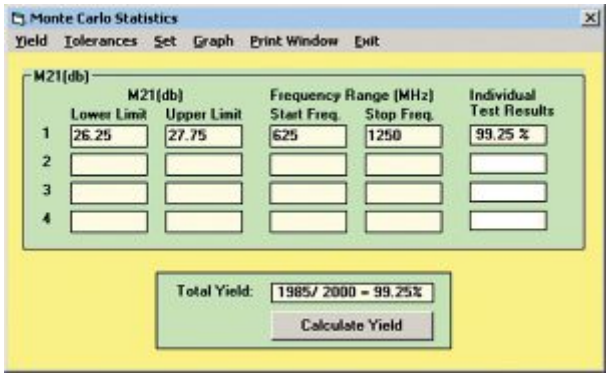

Figure 9: LINC2 statistical yield goals

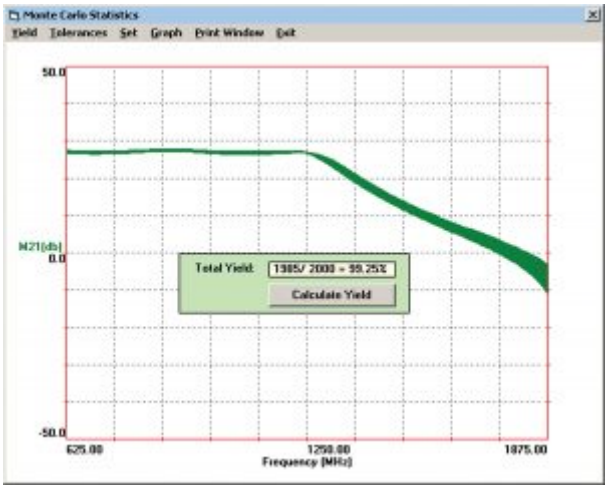

Figure 10: LINC2 Monte Carlo yield analysis

Clicking Calculate Yield performs the yield analysis over the specified number of samples. In this case the sample size was set to 2000. Yields for the individual goals are displayed next to the goal while the total yield is displayed at the bottom of the statistics window (**Figures 9** and **10**). The total yield shows the number of successful results over the total number of trials performed. The percentage of successful trials is also displayed. Checking Show Graph in the Graph menu displays the results for each trial run graphically, as shown in **Figure 10**.

For the two-stage amplifier circuit of **Figure 7**, the yield for two thousand samples is 99.25% for a peak to peak gain variation of no more than 1.5 dB over the octave bandwidth (625 MHz to 1250 MHz). A subsequent Monte Carlo run showed that with only a slight tightening of the dimensional tolerances of the microstrip a 100% yield was produced.

Summary and Conclusions
A design procedure in which circuit synthesis is used to create the initial circuit for subsequent analysis and optimization was presented. A two-stage wideband amplifier circuit, designed using the LINC2 program, demonstrated that virtually complete design automation can be realized when design software integrates circuit synthesis with schematic capture, simulation, optimization and design verification (statistical yield analysis).

Though not included within the scope of this article, the speed and efficiency at which circuit synthesis software can be employed to test a variety of "what if" scenarios should be obvious to the reader. For example, the amplifier design in this article utilized only one of many available distributed input/output matching topologies. However, would the broadband characteristics of ¼ wave stepped-impedance transmission line transformers have enabled greater bandwidth or better return loss over the given band? Or, would a lumped multi-element solution have provided a better match considering the relatively low frequency (625 MHz) at the low end of the band? The answer to these and many other questions can be answered in a matter of seconds with circuit synthesis. The synthesis program automatically creates the circuit schematic and sets up the simulation environment ready for simulation, so the results are immediate.

LINC2 is a high performance, low cost, RF and microwave design and simulation program that includes many value-added features for automating design tasks, including circuit synthesis. More information about LINC2 can be found on the ACS web site at www.appliedmicrowave.com.

Related Posts:

1. **An RF Simulator for Enhanced Cascade System Analysis**

2. **Fast and Efficient RF Amplifier Design Using LINC2 Automated Circuit Synthesis**